Analog CMOS Circuit for Solving Quadratic Programming Problems

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Abstract

This work focuses on creating an analog circuit using complementary metal-oxide semiconductor (CMOS) technology to aid in solving quadratic programming problems (QPP). QPP Circuits using op-amp and operational transconductance amplifiers (OTA) were also investigated. Quadratic programming is type of convex optimization found in the field of control and it entails minimizing a quadratic function subject to constraints. The circuit will ultimately be for control related applications due to the presence of QPPs in this field.

The aim of the research is to design multiple circuits capable of performing some mathematical operation such as addition, integration, or vector-matrix multiplication. Particular attention is paid to using CMOS transistors to realize these circuits given their potential for a VLSI implementation. Specific nodes within the circuit converge towards an equilibrium voltage, in turn providing the values of the optimal vector of optimization variables that minimizes the quadratic program.

Background

Analog Circuits are useful in the field of control because they typically require little power and maintain a relatively high level of accuracy.

Kennedy and Chua proposed a neural network circuit for nonlinear programming problems in a 1998 paper, [1]. Skibik and Adegbege use OTAs and capacitors only to solve an MPC formulated as a quadratic program in a 2018 paper, [2].

A 2020 paper by Paliy, [3], realizes a CMOS current-to-current vector-matrix multiplication (VMM) circuit using gained current mirrors. A similar circuit was developed during the course of the research with the intent to embed it within a larger circuit for quadratic programming problems.

Quadratic Program Problem Definition

Minimize the following quadratic function:

$$f(x) = \frac{1}{2}x^T Hx + x^T q,$$

subject to

$$h(x) = Ax - b = 0,$$

where $x \in \mathbb{R}^n$, $H \in \mathbb{R}^{nxn}$, $A \in \mathbb{R}^{mxn}$, $b \in \mathbb{R}^m$, $q \in \mathbb{R}^n$.
H is a symmetric, positive definite matrix corresponding to the objective function, x is a vector of optimization variables, and the matrix A and vector b form the linear equality constraints.

Neural Network Circuit Model

The Lagrangian is used to find an optimal point of the quadratic program subject to equality constraints:

$$\nabla_x L(x^*, \lambda^*) = -Hx - q - A^T = 0,$$

$$\nabla_\lambda L(x^*, \lambda^*) = Ax - b = 0,$$

A neural network model that converges to an equilibrium value that satisfies the Karush-Kuhn Tucker conditions is employed. Assuming the network is stable, the equilibrium of the system described by the two equations below providing an optimal solution to the quadratic program, [4]:

$$\dot{x} = -Hx - q - A^T x$$

$$\dot{\lambda} = Ax - b$$

References

[1] M.P. Kennedy and L.O. Chua. "Neural networks for nonlinear programming". In:IEEE Transactionson Circuits and Systems35.5 (1988), pp. 554–562
[2] Terrence Skibik and Ambrose A. Adegbege. "An Architecture for Analog VLSI Implementation ofEmbedded Model Predictive Control". In:2018 Annual American Control Conference (ACC). 4676-4681. 2018, pp. 4676–4681
[3] Maksym Paliy et al. "Analog Vector-Matrix Multiplier Based on Programmable Current Mirrors forNeural Network Integrated Circuits". In:IEEE Access8 (2020), pp. 203525–2035377
[4] S. Zhang and A.G. Constantinides. "Lagrange programming neural networks". In:IEEE Transactionson Circuits and Systems II: Analog and Digital Signal Processing39.7 (1992), pp. 441–452

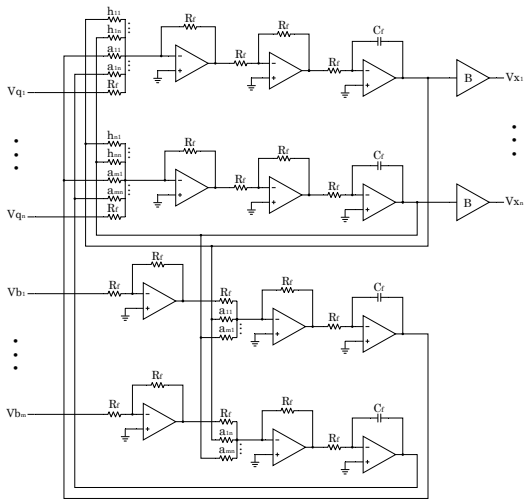
Op-Amp Quadratic Program Setup

The op-amp quadratic program circuit is based on the neural network model in which certain node voltages converge to the solution. The system is described by the following two equations:

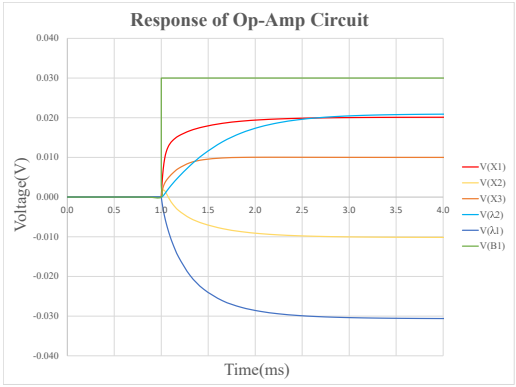
$$\dot{v}_x = -Hv_x - v_q - A^T v_\lambda,$$

$$\dot{v}_\lambda = Av_x - v_b$$

Op-Amp Quadratic Program Circuit



Op-amp Quadratic Program Simulation



Simulation Values:

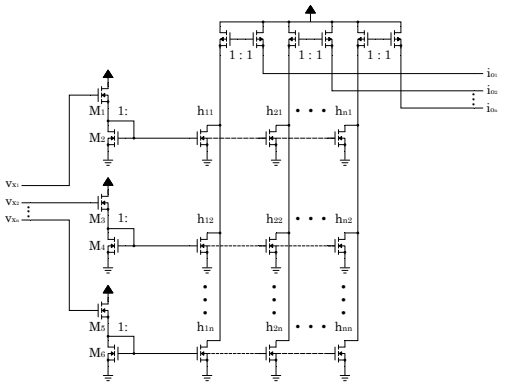
$$H = \begin{pmatrix} 6 & 2 & 1 \\ 2 & 5 & 2 \\ 1 & 2 & 4 \end{pmatrix}; A = \begin{pmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \end{pmatrix}; v_q = \begin{pmatrix} -0.080 \\ -0.030 \\ -0.030 \end{pmatrix}; v_q = \begin{pmatrix} 0.030 \\ 0.000 \end{pmatrix}.$$

CMOS Vector-Matrix Multiplier Setup

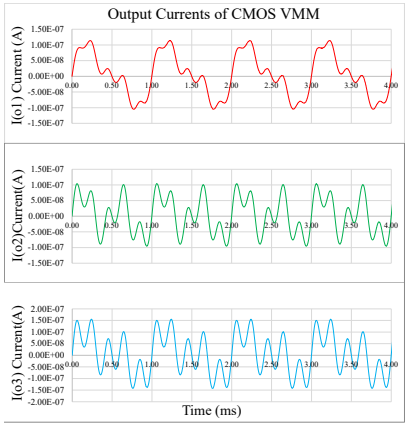
Small-signal gate voltages $v_{x_1}, v_{x_2}, \ldots, v_{x_n}$ are applied to M_1, M_3, and M_5 producing small-signal drain currents which are mirrored with a gain corresponding to the elements in the matrix and summed along a branch via KCL to produce the output currents $i_{o_1}, i_{o_2}, \ldots, i_{o_n}$.

$$\begin{pmatrix} i_{o_1} \\ i_{o_2} \\ \vdots \\ i_{o_n} \end{pmatrix} = \frac{1}{2} g_m \begin{pmatrix} h_{11} & h_{12} & \cdots & h_{1n} \\ h_{21} & h_{22} & \cdots & h_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ h_{n1} & h_{n2} & \cdots & h_{nn} \end{pmatrix} \begin{pmatrix} v_{x_1} \\ v_{x_2} \\ \vdots \\ v_{x_n} \end{pmatrix}$$

CMOS Vector-Matrix Multiplier Circuit



CMOS Vector-Matrix Multiplier Simulation



Simulation Values:

$$H = \begin{pmatrix} 4 & 2 & 1 \\ 1 & 3 & 2.5 \\ 3 & 3 & 4 \end{pmatrix}; v_x = 20 \times 10^{-3} \begin{pmatrix} \sin(1000t) \\ \sin(2000t) \\ \sin(5000t) \end{pmatrix}; g_m = 20.7 \times 10^{-9} \frac{A}{V}$$

Conclusion

This research successfully realized an op-amp circuit capable of solving quadratic programs subject to linear equality constraints as well as a CMOS voltage-to-voltage vector-matrix multiplier circuit. Simulation results demonstrate the potential of using a transistor level circuit to perform vector-matrix multiplication and using analog circuits for solving QPPS with a relatively high degree of accuracy. Future work entails embedding the CMOS vector-matrix multiplier in an operational transconductance amplifier circuit for solving QPPs as well as biasing the MOSFETs in the subthreshold region.