Analog CMOS Circuit for Solving Quadratic Programming Problems

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Abstract

This work focuses on creating an analog circuit using complementary metal-oxide semiconductor (CMOS) technology to aid in solving quadratic programming problems (QPP). QPP Circuits using op-amp and operational transconductance amplifiers (OTA) were also investigated. Quadratic programming is type of convex optimization found in the field of control and it entails minimizing a quadratic function subject to constraints. The circuit will ultimately be for control related applications due to the presence of QPPs in this field.

The aim of the research is to design multiple circuits capable of performing some mathematical operation such as addition, integration, or vector-matrix multiplication. Particular attention is paid to using CMOS transistors to realize these circuits given their potential for a VLSI implementation. Specific nodes within the circuit converge towards an equilibrium voltage, in turn providing the values of the optimal vector of optimization variables that minimizes the quadratic program.

Background

Analog Circuits are useful in the field of control because they typically require little power and maintain a relatively high level of accuracy. Kennedy and Chua proposed a neural network circuit for nonlinear programming problems in a 1998 paper, [1]. Skibik and Adegbege use OTAs and capacitors only to solve an MPC formulated as a quadratic program in a 2018 paper, [2]. A 2020 paper by Paliv, [3], realizes a CMOS current-to-current vector-matrix multiplication (VMM) circuit using gained current mirrors. A similar circuit was developed during the course of the research with the intent to embed it within a larger circuit for quadratic programming problems.

Quadratic Program Problem Definition

Minimize the following quadratic function:

\[ f(x) = \frac{1}{2} x^T H x + x^T q, \]

subject to

\[ Ax = b = 0, \]

where \( x \in \mathbb{R}^n \), \( H \in \mathbb{R}^{m \times n}, A \in \mathbb{R}^{m \times n}, q \in \mathbb{R}^m \).

\( H \) is a symmetric, positive definite matrix corresponding to the objective function, \( x \) is a vector of optimization variables, and the matrix \( A \) and vector \( b \) form the linear equality constraints.

Neural Network Circuit Model

The Lagrangian is used to find an optimal point of the quadratic program subject to equality constraints:

\[ \nabla_q L(x^*, \lambda^*) = -Hx - q - ATx = 0, \]
\[ \nabla_x L(x^*, \lambda^*) = Ax - b = 0. \]

A neural network model that converges to an equilibrium value that satisfies the Karush-Kuhn-Tucker conditions is employed. Assuming the network is stable, the equilibrium of the system described by the two equations below providing an optimal solution to the quadratic program, [4]:

\[ \dot{x} = -Hx - q - ATx, \]
\[ \dot{\lambda} = Ax - b. \]

Reference:


Conclusion

This research successfully realized an op-amp circuit capable of solving quadratic programs subject to linear equality constraints as well as a CMOS voltage-to-voltage vector-matrix multiplier circuit. Simulation results demonstrate the potential of using a transistor level circuit to perform vector-matrix multiplication and using analog circuits for solving QPPs with a relatively high degree of accuracy. Future work entails embedding the CMOS vector-matrix multiplier in an operational transconductance amplifier circuit for solving QPPs as well as biasing the MOSFETs in the subthreshold region.